AMENDMENT TO THE CLAIMS

This listing of claims is a copy of all pending claims identifies the status of each claim, and replaces all prior versions and listings of claims in the application.

Listing of Claims

1. (Currently amended) A power clamp for an integrated circuit, comprising:

a transistor network composed of a first nFET and a second nFET ~~a first and second transistor~~ respectfully connected in series with one another between a voltage source and a ground, and a third nFET connected in series with the first nFET and the second nFET between the voltage source and the ground;

a bias network configured to bias a gate of the first transistor of the transistor network to a portion of a voltage value of the voltage source; and

a trigger network configured to communicate the occurrence of an electrostatic discharge event to the gate of the second transistor of the transistor network.

Claims 2 and 3. (Canceled).

4. (Previously presented) A power clamp for an integrated circuit, comprising:

a transistor network connected between a voltage source and a ground;

a bias network configured to bias a gate of a first transistor of the transistor network to a portion of a voltage value of the voltage source; and

a trigger network configured to communicate the occurrence of an electrostatic discharge event to the gate of a second transistor of the transistor network,

wherein the transistor network comprises a first nFET and a second nFET

connected in series with one another between the voltage source and a ground,

wherein the transistor network further comprises a third nFET connected in series with the first nFET and the second nFET between the voltage source and the ground, and

wherein the bias network further comprises a voltage divider configured to communicate a portion of the voltage from the voltage source to the gate of the first transistor and a gate of the third nFET.

5. (Original) The power clamp of claim 1, wherein the bias network comprises a voltage divider configured to communicate a portion of the voltage from the voltage source to the gate of the first transistor.

6. (Original) The power clamp of claim 1, wherein the trigger network comprises a resistor and a capacitor configured to filter out non-electrostatic discharge events from the gate of the second transistor.

7. (Previously presented) A power clamp for an integrated circuit, comprising:

at least an upper and a lower nFET respectively connected in series with one another between a pair of power supply rails from a higher potential to a lower potential;

a voltage divider configured to bias a gate of the upper nFET to a prescribed value; and

a low frequency filter connected to a gate of the lower nFET and configured to filter out low frequency signals between at least one power supply rail and the gate of

the lower nFET.

8. (Original) The power clamp of claim 7, wherein the gate of the upper nFET is biased to a prescribed fraction of a voltage between the pair of power supply rails.

9. (Previously presented) The power clamp of claim 7, wherein the voltage divider is connected between the pair of power supply rails and comprises at least one bias network.

10. (Original) The power clamp of claim 9, wherein the voltage divider comprises at least one resistor.

11. (Original) The power clamp of claim 7, wherein the low frequency filter communicates with a source and a drain of the lower nFET.

Claims 12. – 20. (Canceled).